

**FIG. 1**

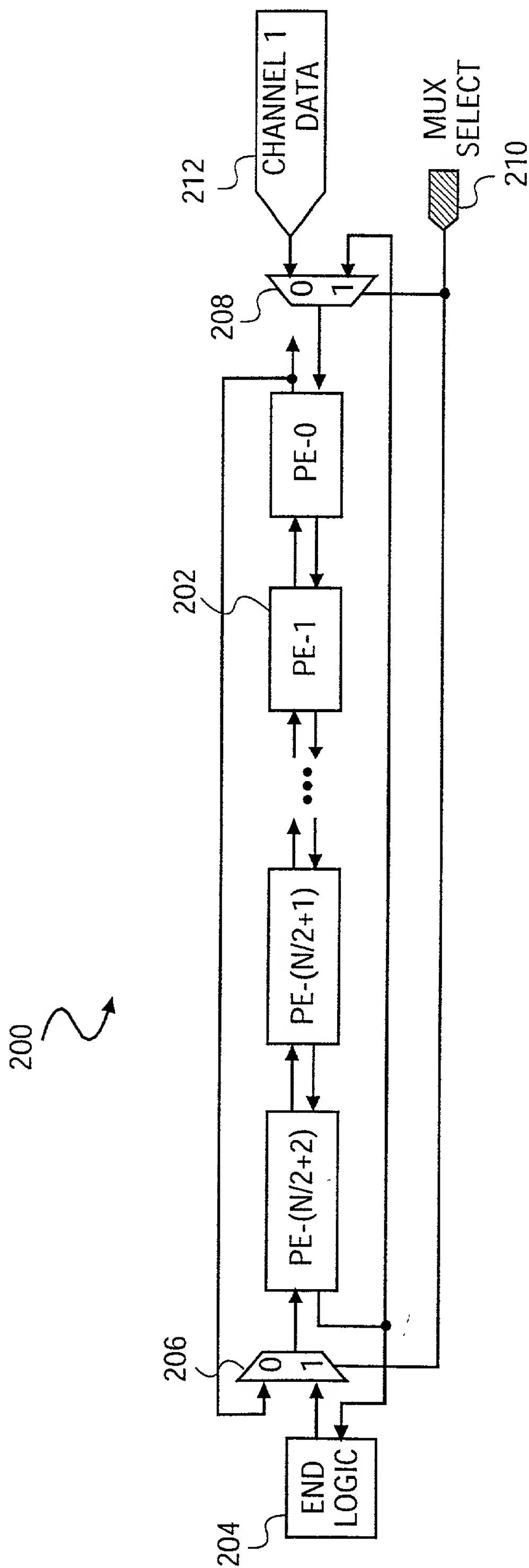


FIG. 2



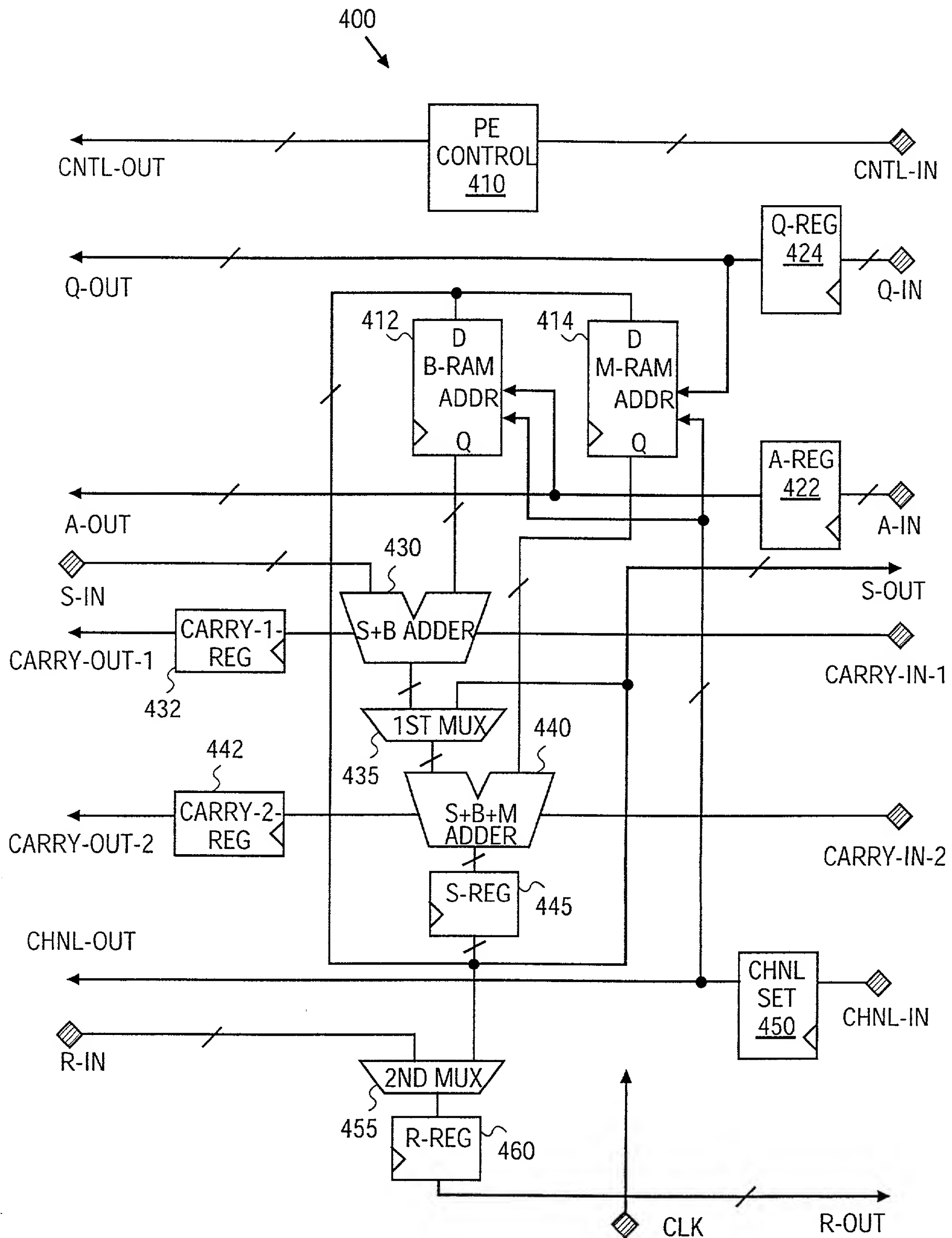
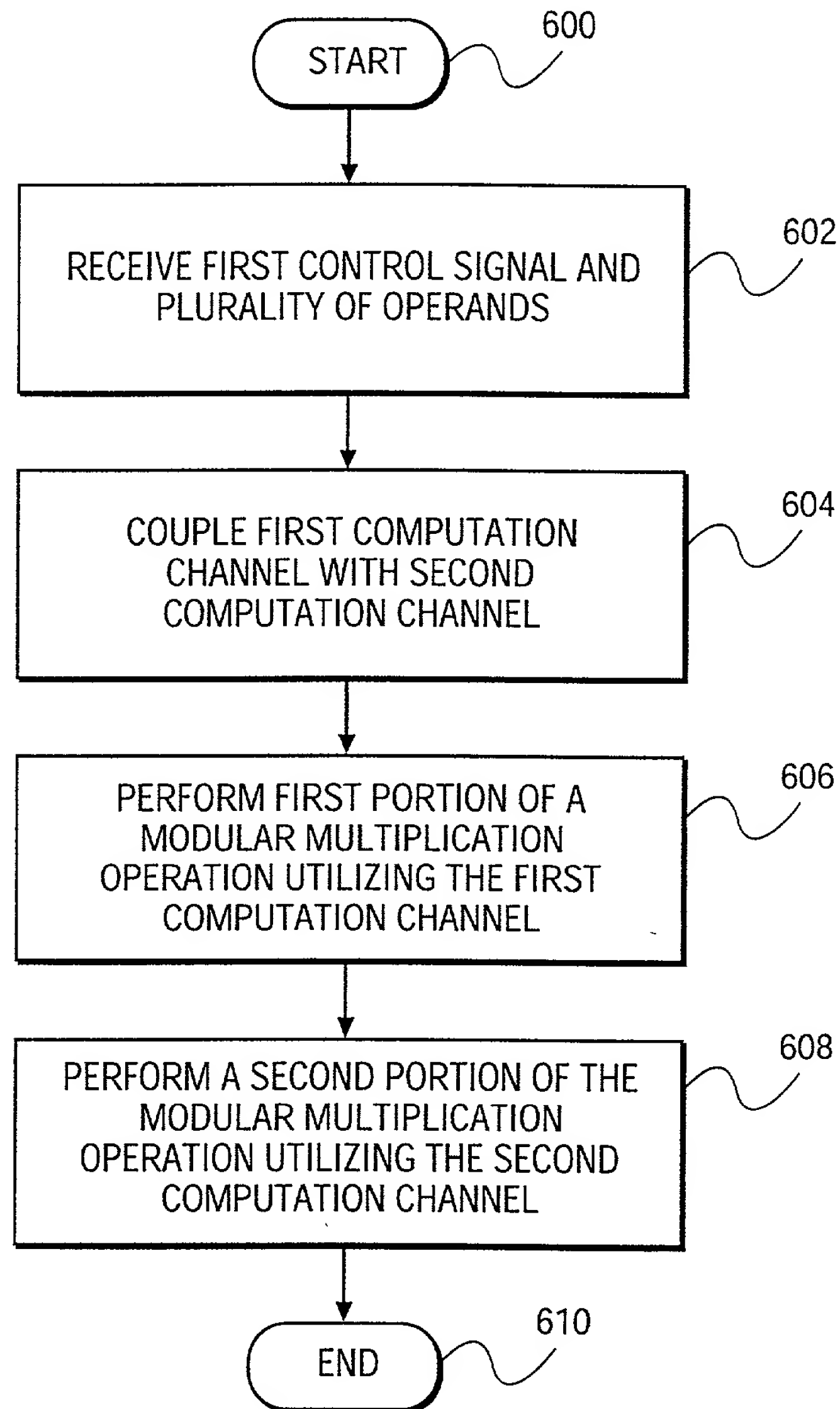


FIG. 4

CYCLE	MUX SELECT	END LOGIC	PE-6	PE-5	PE-4	PE-3	PE-2	PE-1	PE-0	INPUT REGS
1	0									
2	1								0	
3	0							1		
4	1						2		0	
5	0					3		1		
6	1				4		2		0	
7	0			5		3		1		
8	1		6		4		2		0	
9	0			5		3		1	7	
10	1		6		4		2	8	0	
11	0			5		3	9	1	7	
12	1		6		4	10	2	8	0	
13	0			5	11	3	9	1	7	
14	1		6	12	4	10	2	8	0	
15	0		13	5	11	3	9	1	7	
16	1		6	12	4	10	2	8	0	
17	0		13	5	11	3	9	1	7	
18	1		6	12	4	10	2	8	0	
19	0		13	5	11	3	9	1	7	
20	1		6	12	4	10	2	8	0	

FIG. 5



**FIG. 6**